CLAIMS

1. A fault detecting method for a semiconductor integrated circuit, characterized in that:

a fault list corresponding to information on sites of a semiconductor integrated circuit where a fault is likely to occur or information required to reduce faults is used to perform detection for faults in said semiconductor integrated circuit.

2. The fault detecting method for a semiconductor integrated circuit according to claim 1, wherein in fault detection, faults that are difficult to detect are omitted from the fault list before detection is performed for faults in the semiconductor integrated circuit using a remaining part of the fault list.

3. The fault detecting method for a semiconductor integrated circuit according to claim 1, wherein the fault list contains data on likelihood of each fault.

4. The fault detecting method for a semiconductor integrated circuit according to claim 3, wherein detection is performed for faults in the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

5. The fault detecting method for a semiconductor integrated circuit according to claim 3, wherein the faults are weighted with their likelihood to determine a fault coverage for a fault detection.

6. The fault detecting method for a semiconductor integrated circuit according to claim 5, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

7. The fault detecting method for a semiconductor integrated circuit according to claim 4, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

8. The fault detecting method for a semiconductor integrated circuit according to claim 4, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

9. The fault detecting method for a semiconductor integrated circuit according to claim 4, wherein the faults are ordered or weighted with their likelihood using a database

for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

10. The fault detecting method for a semiconductor integrated circuit according to claim 6, wherein a fault coverage that can be obtained when detecting each fault is calculated and faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

11. The fault detecting method for a semiconductor integrated circuit according to claim 6, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

12. A fault detecting method for a semiconductor integrated circuit, characterized in that:

detection is performed for faults in a semiconductor integrated circuit to create a fault list corresponding to information on sites of the semiconductor integrated circuit where a fault is likely to occur or information required to reduce faults so that this fault list can be used to perform detection for faults in said semiconductor integrated circuit.

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13. The fault detecting method for a semiconductor integrated circuit according to claim 12, wherein in fault detection, faults that are difficult to detect are omitted from a fault list before detection is performed for faults in the semiconductor integrated circuit using a remaining part of the fault list.

14. The fault detecting method for a semiconductor integrated circuit according to claim 12, wherein the fault list contains data on likelihood of each fault.

15. The fault detecting method for a semiconductor integrated circuit according to claim 14, wherein detection is performed for faults in the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

16. The fault detecting method for a semiconductor integrated circuit according to claim 14, wherein the faults are weighted with their likelihood to determine a fault coverage for a fault detection.

17. The fault detecting method for a semiconductor integrated circuit according to claim 16, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

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18. The fault detecting method for a semiconductor integrated circuit according to claim 15, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

19. The fault detecting method for a semiconductor integrated circuit according to claim 15, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

20. The fault detecting method for a semiconductor integrated circuit according to claim 15, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

21. The fault detecting method for a semiconductor integrated circuit according to claim 17, wherein a fault coverage that can be obtained when detecting each fault is calculated and faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

22. The fault detecting method for a semiconductor integrated circuit according to claim 17, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

23. A layout method for a semiconductor integrated circuit, characterized in that:

a fault list corresponding to information on sites of a semiconductor integrated circuit where a fault is likely to occur or information required to reduce faults is used to perform mask layout and wiring for said semiconductor integrated circuit.

24. The layout method for a semiconductor integrated circuit according to claim 23, wherein the fault list contains data on likelihood of each fault.

25. The layout method for a semiconductor integrated circuit according to claim 24, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

26. The layout method for a semiconductor integrated circuit according to claim 24, wherein the faults are weighted with their likelihood to determine a fault coverage for the

mask layout and wiring for the semiconductor integrated circuit.

27. The layout method for a semiconductor integrated circuit according to claim 26, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

28. The layout method for a semiconductor integrated circuit according to claim 25, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

29. The layout method for a semiconductor integrated circuit according to claim 25, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

30. The layout method for a semiconductor integrated circuit according to claim 25, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

31. The layout method for a semiconductor integrated circuit according to claim 27, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

32. The layout method for a semiconductor integrated circuit according to claim 27, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

33. A layout method for a semiconductor integrated circuit, characterized in that:

detection is performed for faults in a semiconductor integrated circuit to create a fault list indicating information on sites of a semiconductor where a fault is likely to occur or information required to reduce faults so that this fault list can be used to perform mask layout and wiring for said semiconductor integrated circuit.

34. The layout method for a semiconductor integrated circuit according to claim 33, wherein the fault list contains data on likelihood of each fault.

35. The layout method for a semiconductor integrated circuit according to claim 34, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

36. The layout method for a semiconductor integrated circuit according to claim 34, wherein the faults are weighted with their likelihood to determine a fault coverage for the mask layout and wiring for the semiconductor integrated circuit.

37. The layout method for a semiconductor integrated circuit according to claim 36, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

38. The layout method for a semiconductor integrated circuit according to claim 35, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

39. The layout method for a semiconductor integrated circuit according to claim 35, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated

circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

40. The layout method for a semiconductor integrated circuit according to claim 35, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

41. The layout method for a semiconductor integrated circuit according to claim 37, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

42. The layout method for a semiconductor integrated circuit according to claim 37, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

43. A layout method for a semiconductor integrated circuit, characterized in that:

faults that are difficult to detect are omitted from a fault list before mask layout and wiring are performed based

on the remaining part of the fault list for the semiconductor integrated circuit.

44. The layout method for a semiconductor integrated circuit according to claim 43, wherein the fault list contains data on likelihood of each fault.

45. The layout method for a semiconductor integrated circuit according to claim 44, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

46. The layout method for a semiconductor integrated circuit according to claim 44, wherein the faults are weighted with their likelihood to determine a fault coverage for the mask layout and wiring for the semiconductor integrated circuit.

47. The layout method for a semiconductor integrated circuit according to claim 46, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

48. The layout method for a semiconductor integrated circuit according to claim 45, wherein the faults are ordered or weighted with their likelihood based on mask information

obtained from a layout device for laying out the semiconductor integrated circuit.

49. The layout method for a semiconductor integrated circuit according to claim 45, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

50. The layout method for a semiconductor integrated circuit according to claim 45, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

51. The layout method for a semiconductor integrated circuit according to claim 47, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

52. The layout method for a semiconductor integrated circuit according to claim 47, wherein the fault coverage is calculated while carrying out a process for each fault

detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.